IN THE CLAIMS:

1. A chemical-mechanical polishing process comprising the steps of:

chemically mechanically polishing a gap fill material stopping on a first film;

stripping the first film to expose a second film;

after exposing the second film, chemically mechanically polishing the gap fill material stopping on a third film.

2. The method of claim 1, wherein said first and third film comprise the same material.

3. The method of claim 1, wherein said first film and said third film comprise silicon nitride.

4. The method of claim 3, wherein the second film comprises silicon dioxide.

5. The method of claim 1, wherein the third film has a thickness in the range of 30-50 nm.

6. The method of claim 1, wherein said gap fill material forms a shallow trench isolation structure.

7. A method of fabricating an integrated circuit, comprising the steps of:

depositing a first film over a semiconductor body;

depositing a second film over the first film;

depositing a third film over the second film;

patterning and etching said first film, second film and third film;

forming a gap in said semiconductor body;

filling said gap with a gap fill material;

chemically mechanically polishing the gap fill material stopping on said first film;

stripping said first film selectively with respect to the second film; and

chemically mechanically polishing the gap fill material stopping on the third film.

8. The method of claim 7, wherein said first and third film comprise the same material.

9. The method of claim 7, wherein said first film and said third film comprise silicon nitride.

10. The method of claim 9, wherein the second film comprises silicon dioxide.

11. The method of claim 7, wherein the third film has a thickness in the range of 30-50 nm.

12. The method of claim 7, wherein said gap fill material forms a shallow trench isolation structure.

13. The method of claim 7, wherein said step of depositing the gap fill material comprises chemical vapor deposition.

14. The method of claim 7, wherein said step of depositing the gap fill material comprises high density plasma deposition of silicon dioxide.

15. The method of claim 7, wherein said step of forming a gap in the semiconductor body etches metal leads in an interconnect layer of the semiconductor body.

16. The method of claim 7, wherein said step of forming a gap in the semiconductor body etches wordlines in a DRAM process.

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